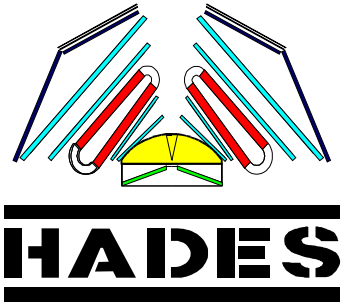
Accurate charge measurement of fast signals via FPGA* based TDC's

Wolfgang Koenig, Jerzy Pietraszko, Michael Traxler
Joint venture of the Hades Collaboration & the Dep. of Experiment-Elektronik @ GSI



Menu:

- Concept
- Amplifier
- Integrator
- First results
- Application for HADES Veto detector
- New FPGA based TDC concept
- First Results
- Summary & outlook

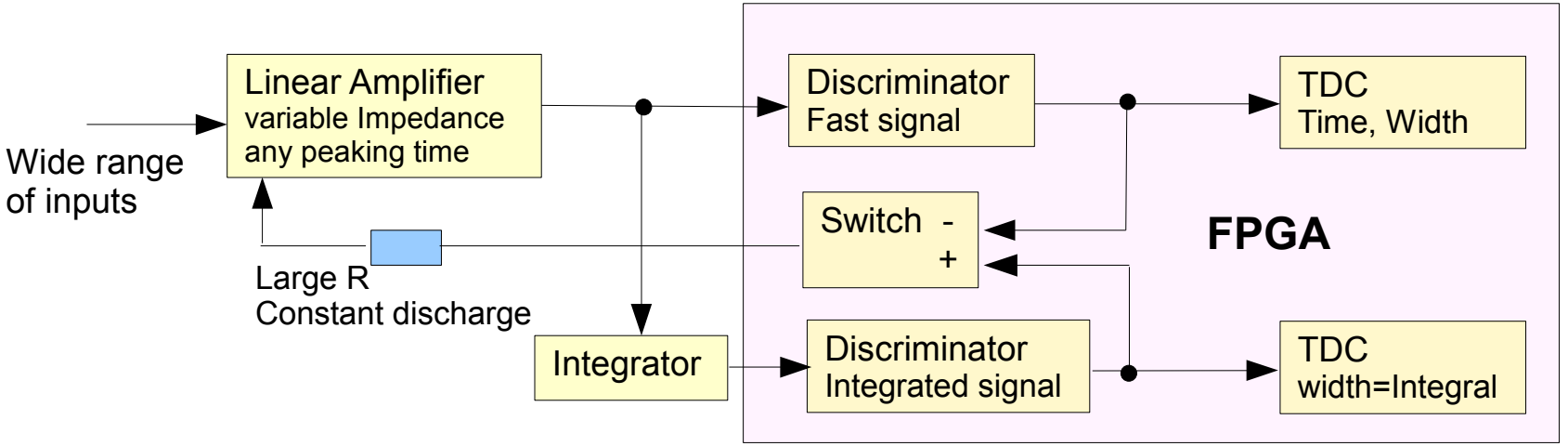
GSI

HELMHOLTZ GEMEINSCHAFT

*Field Programmable Gate Array (AND/Or/Not Logic + FlipFlops + fancy interfaces + ...)

The basic concept:

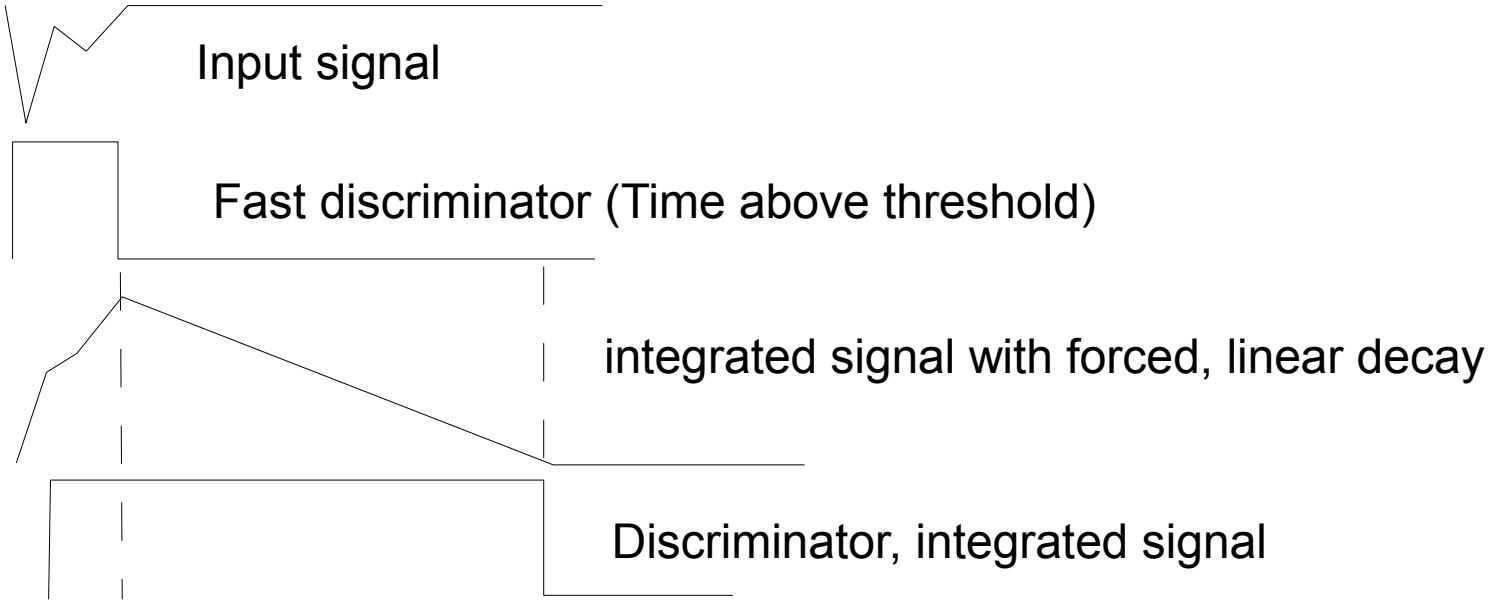
general purpose (Driftchambers, straw tubes, PM's, Diamonds)



keep **i**t **s**mall and **s**imple
Minimum: 2 resistors, 1 capacitor

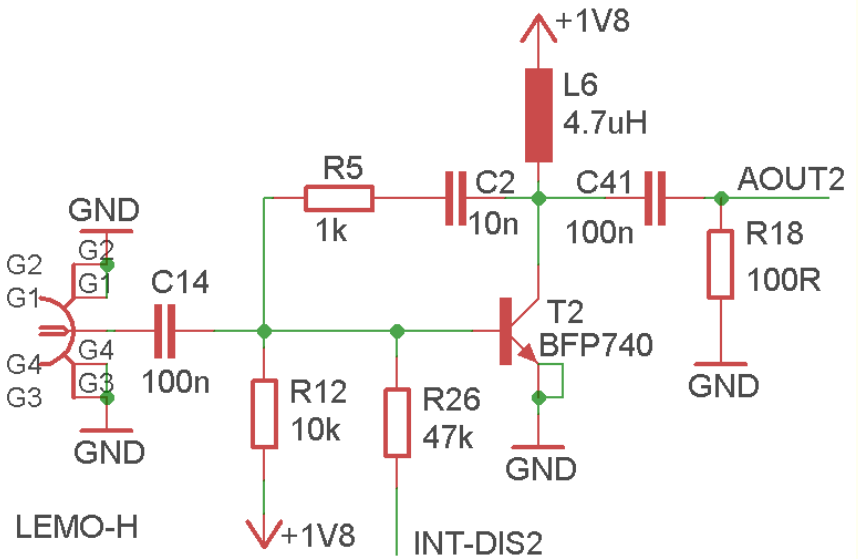
Complex c**om**mercial **e**lement

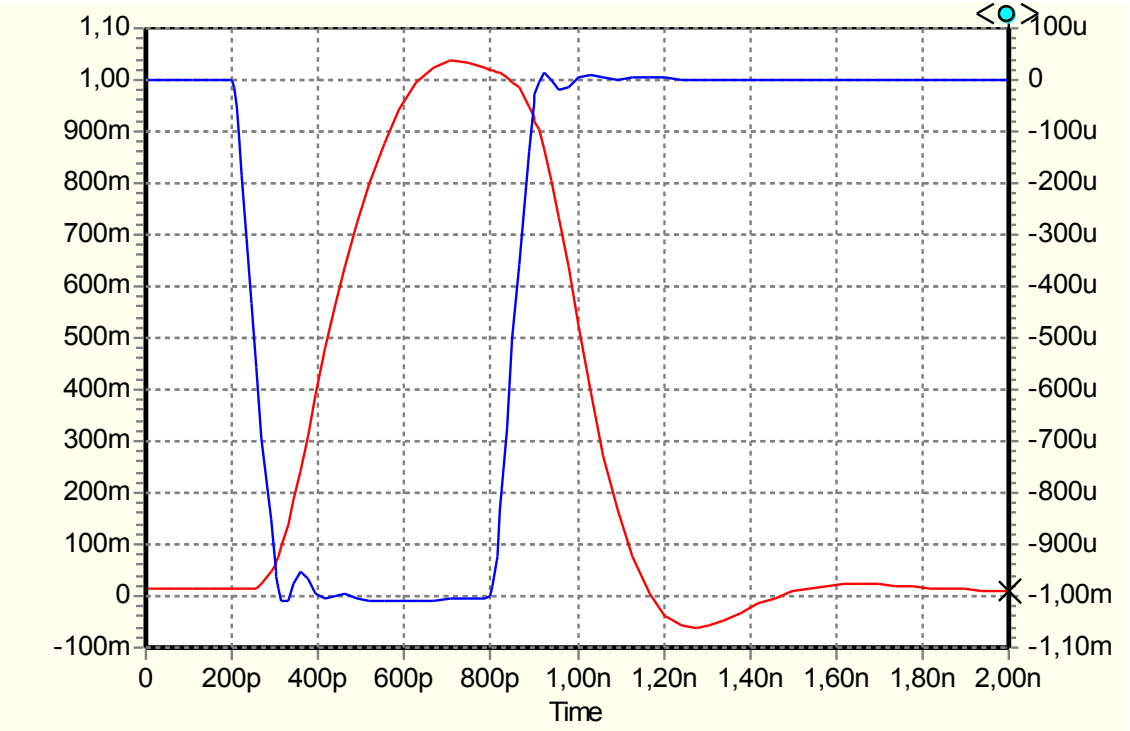
come & kiss

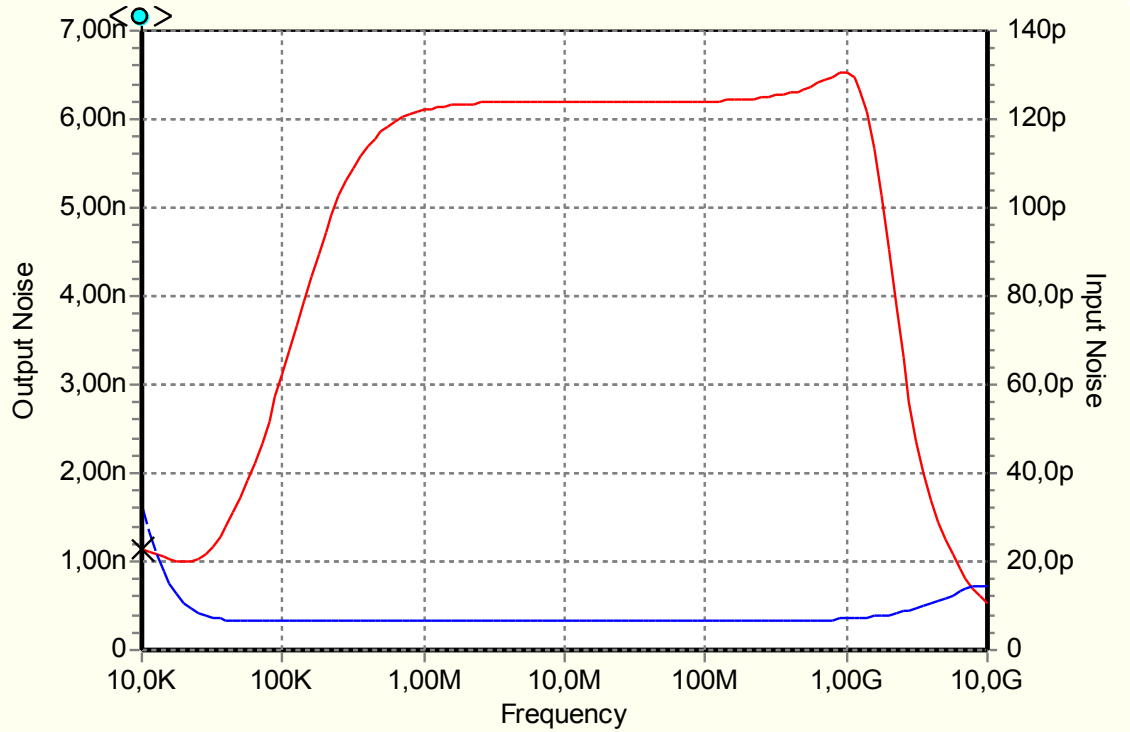


Fast amplifier

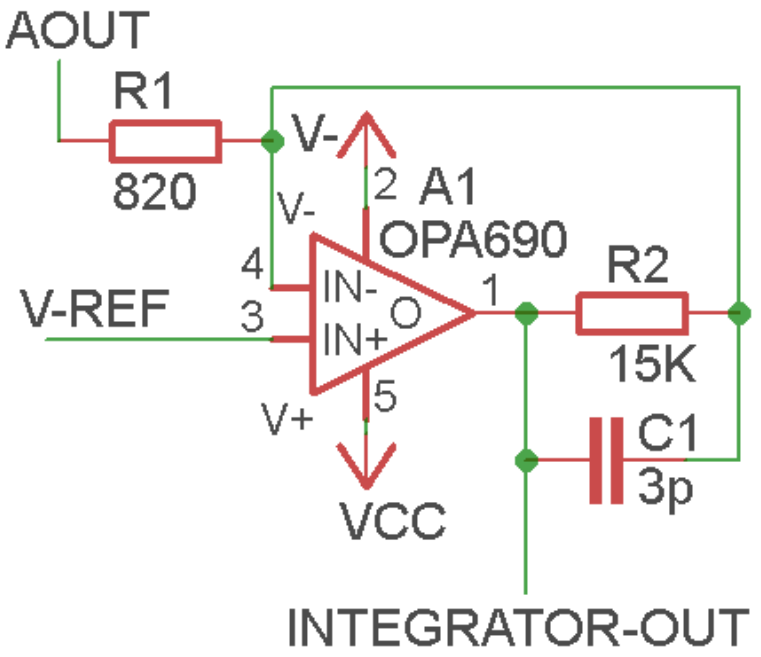
- Low noise: Noise figure: **0.5@1.8GHz**
- Rise time: **240 ps** (100 ps input)
- Fall time: **210 ps** (100ps input)
- Transition frequency: **42 GHz**
- Voltage Gain: **20** (50 Ohm in, 100 Ohm out)

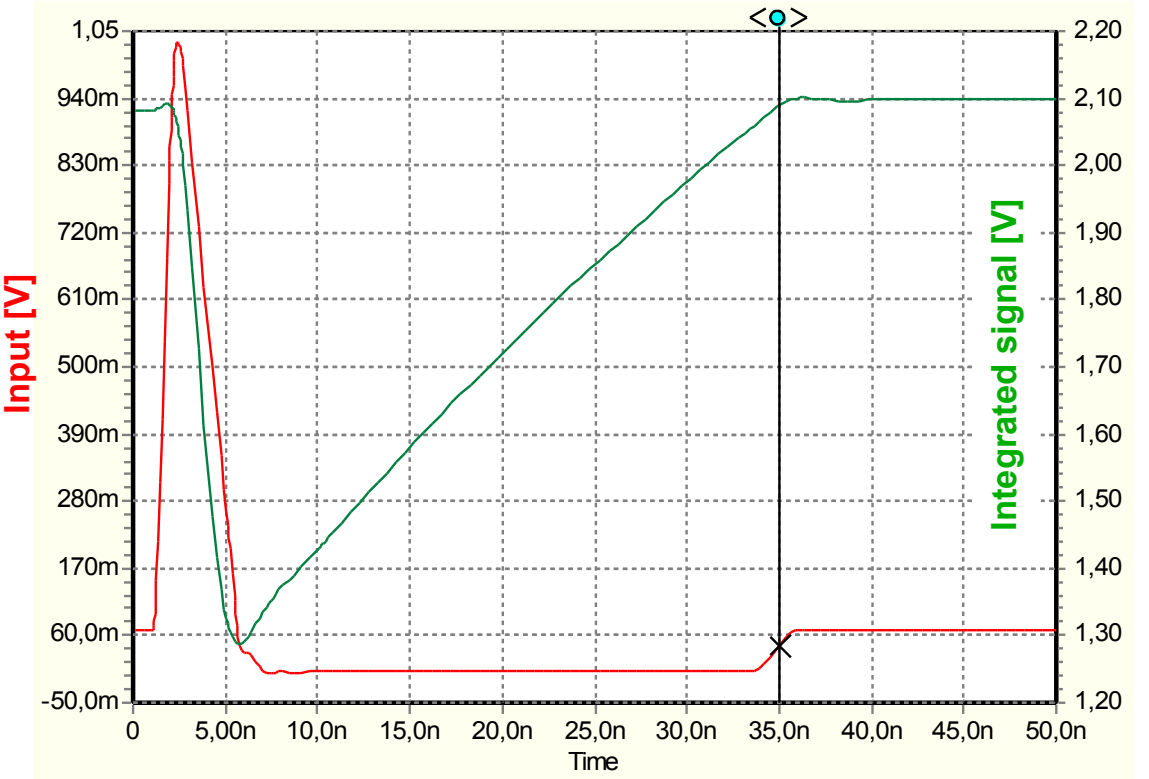






Simple-most integrator

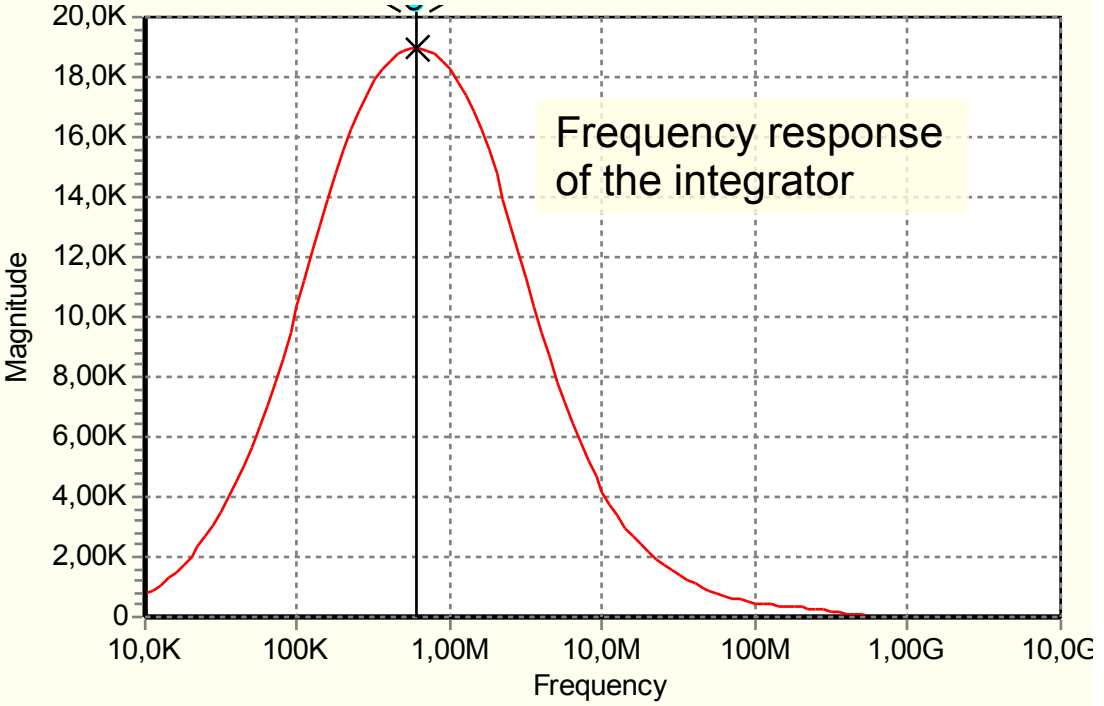




High sensitivity (high gain) for low frequencies:
low frequency noise dominates resolution
Not a spectroscopy amplifier

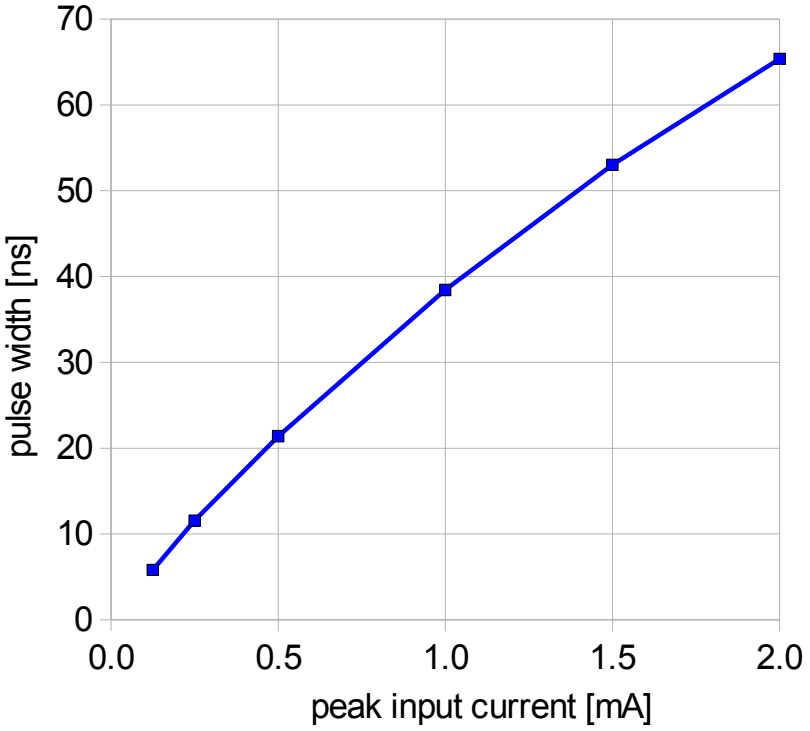
Advantage:

- Short cycle time ~50 ns ⇨ High rate capability
- Triggered baseline-restorer: no rate dependent trigger threshold due to triggered feedback

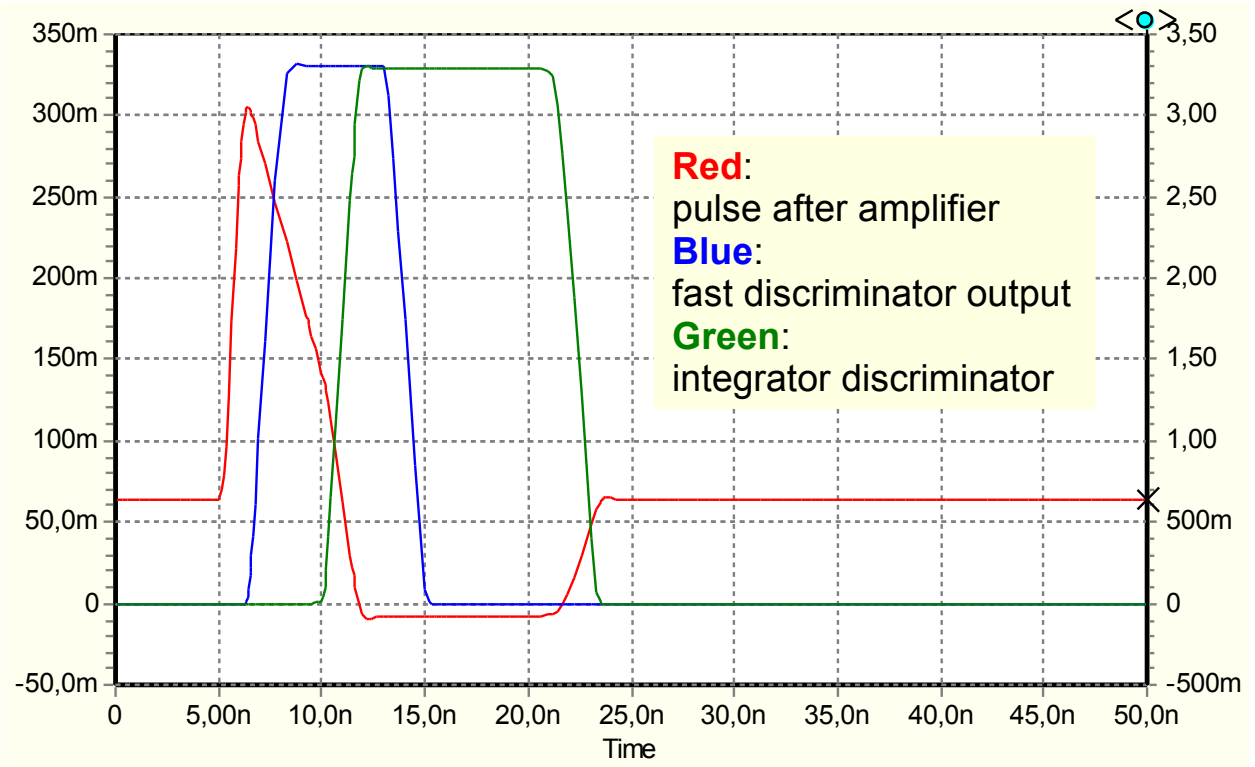


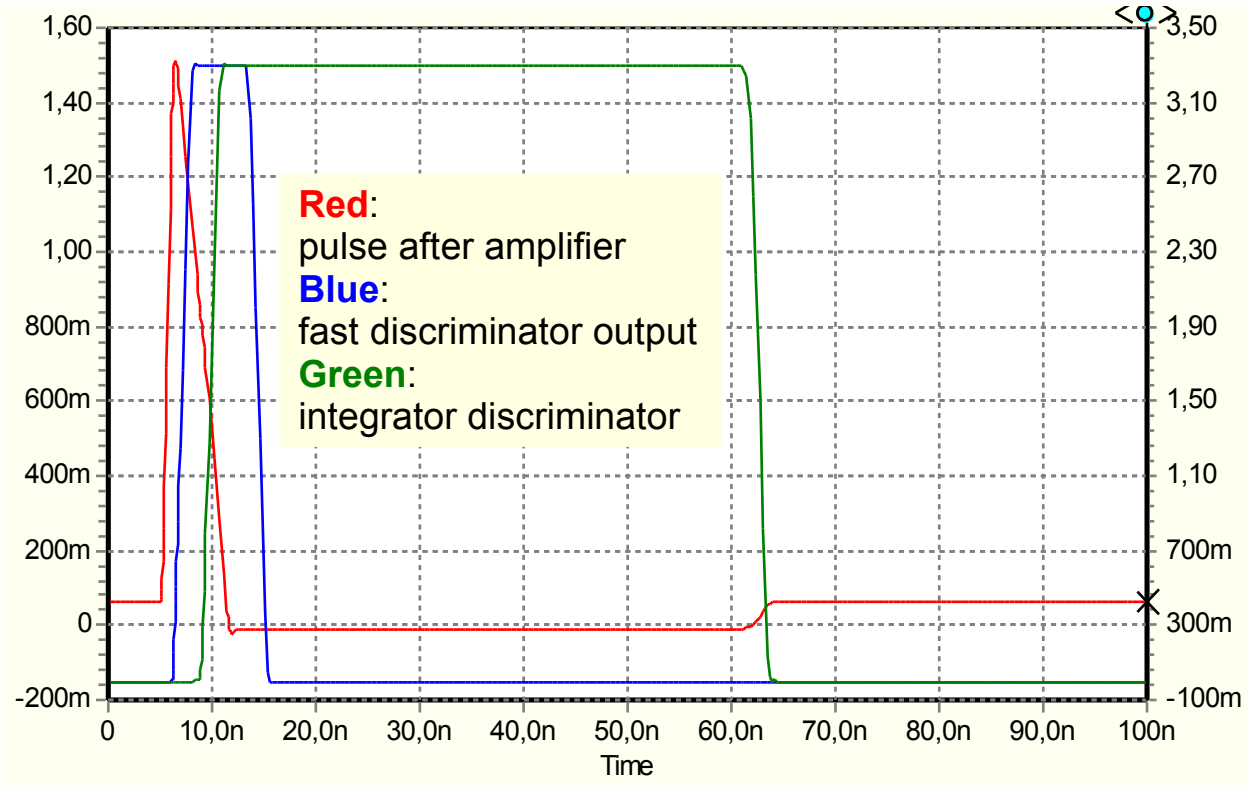
Simulation with discrete components

Risetime: **1ns**
Fall time: **5ns**
Pulse height:
Top: 0.25mA
Bottom: 1.5 mA



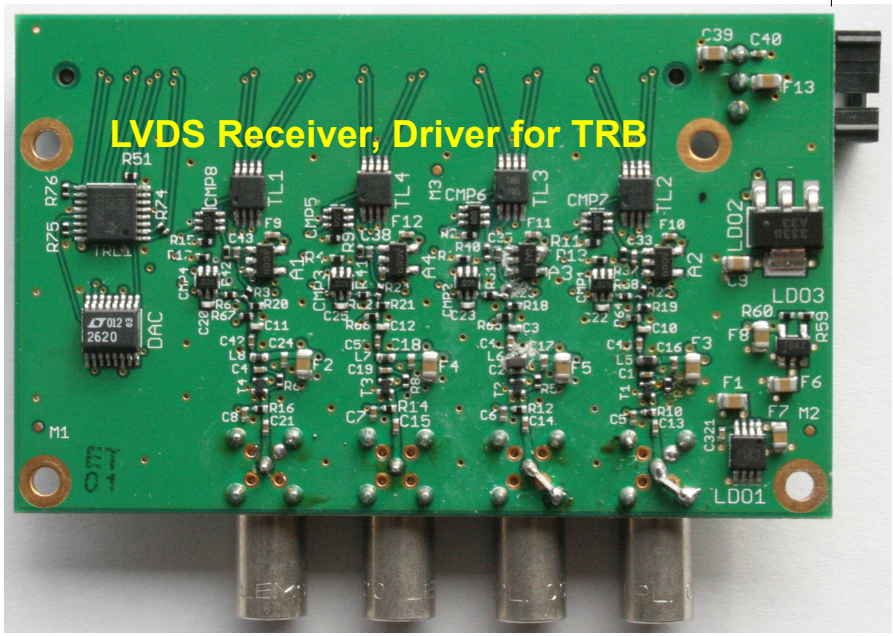
Non-linear amplifier response,
dynamic range about 10 -100
depending on signal width

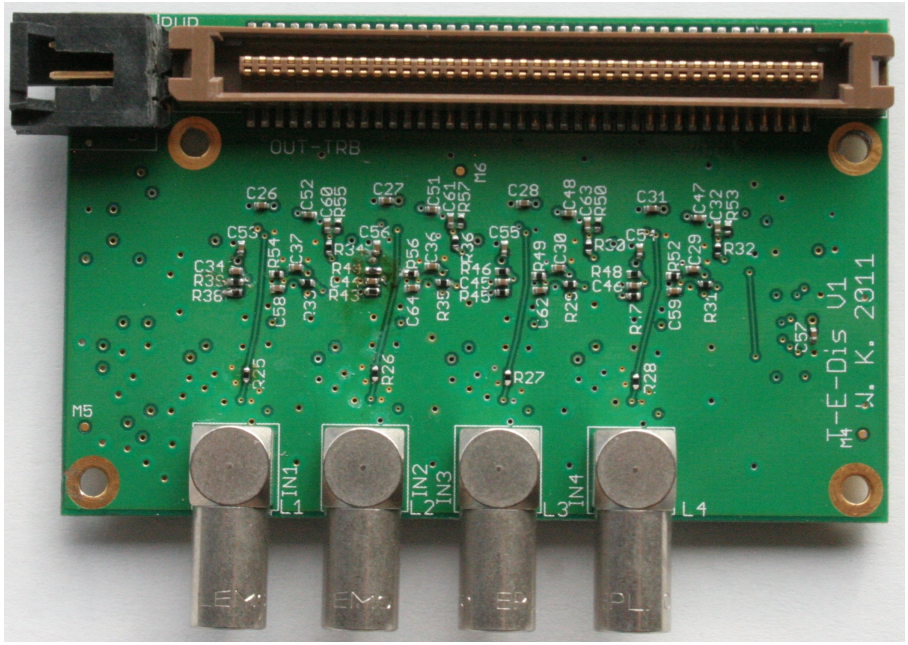




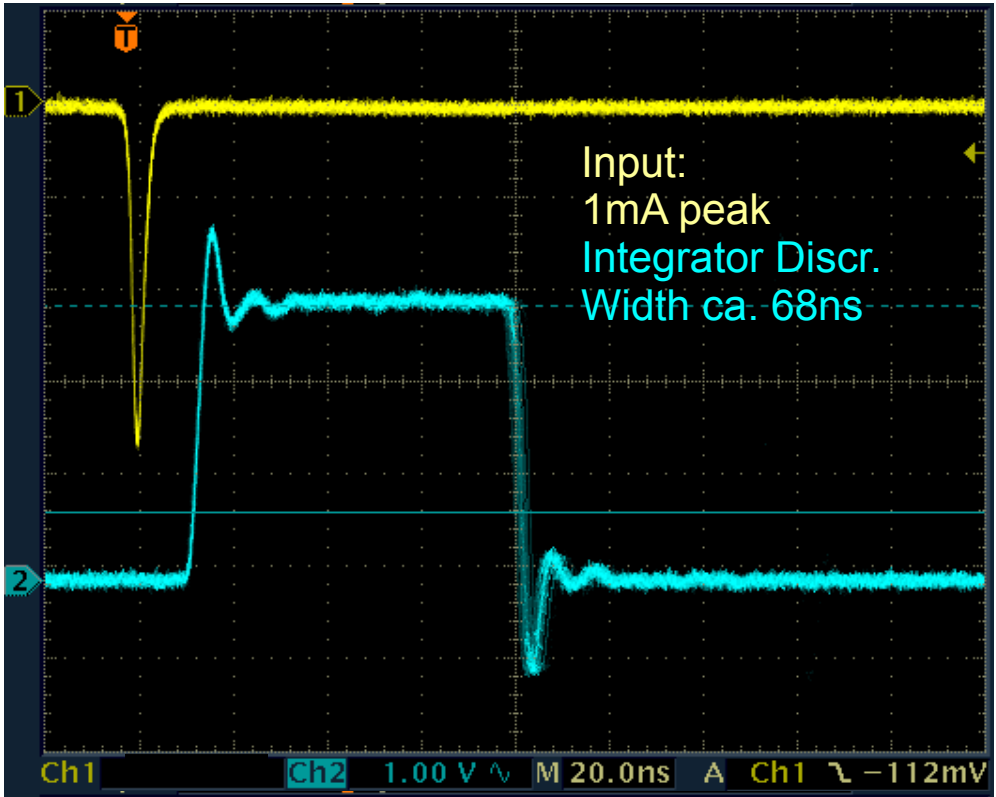
Prototype Board (4 channels) for TRB 2

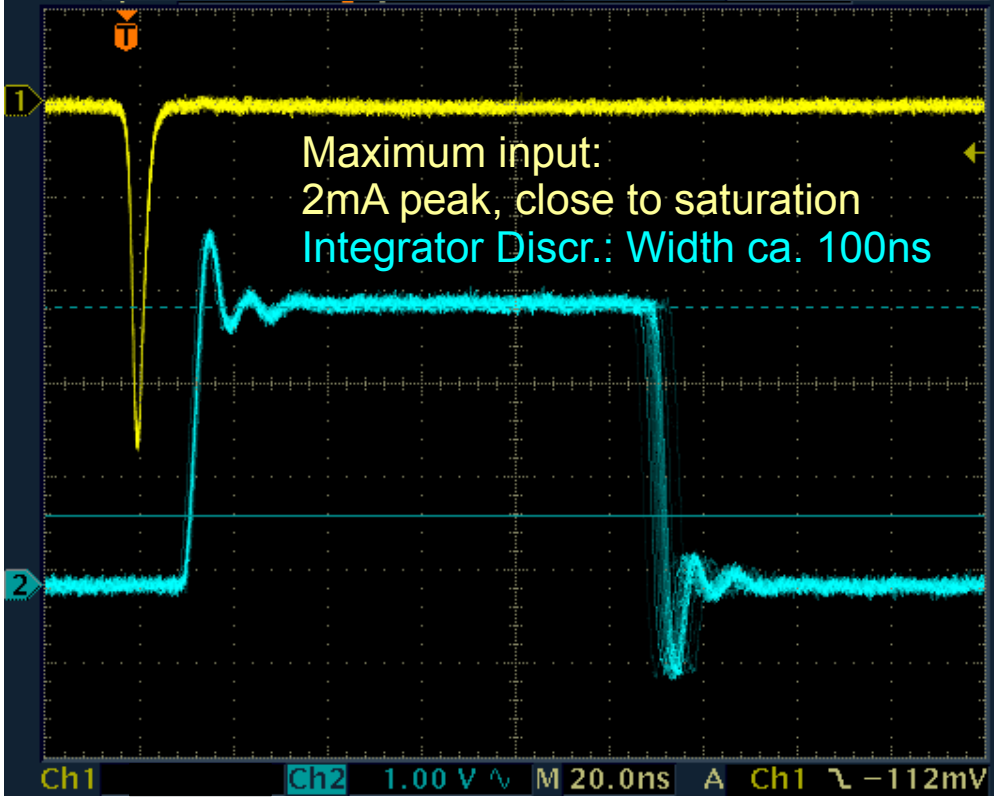
73 mm





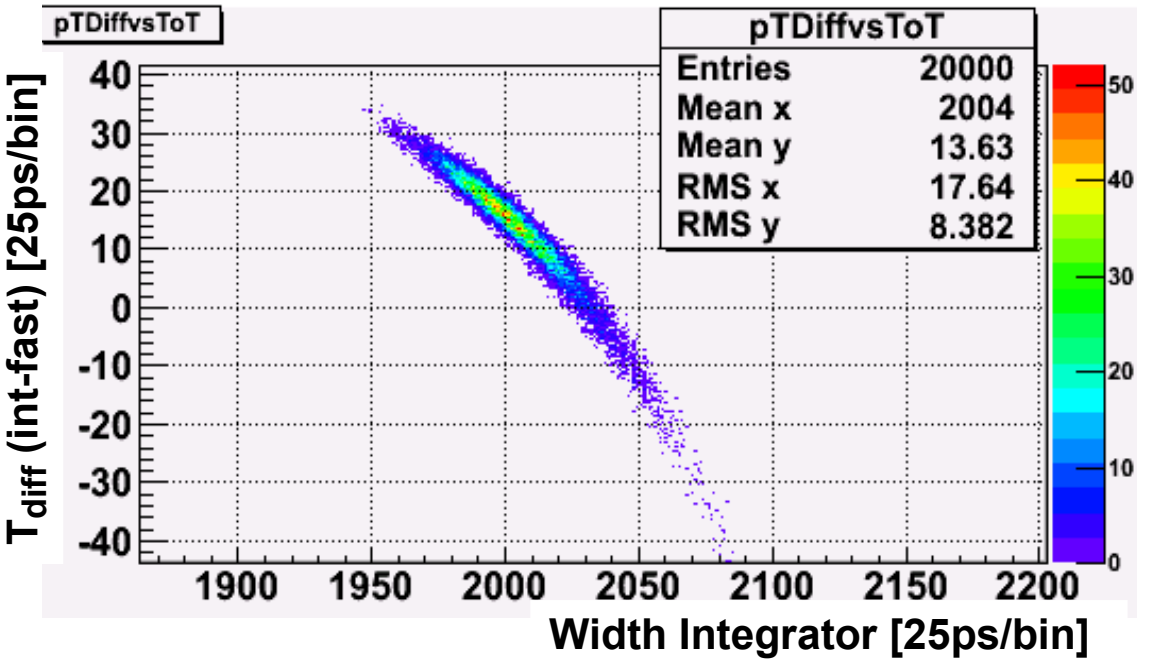
Size determined by connectors and TRB 2 infrastructure





First Results

Pulser t_{rise} = 1.5ns , t_{fall} = 2.5 ns

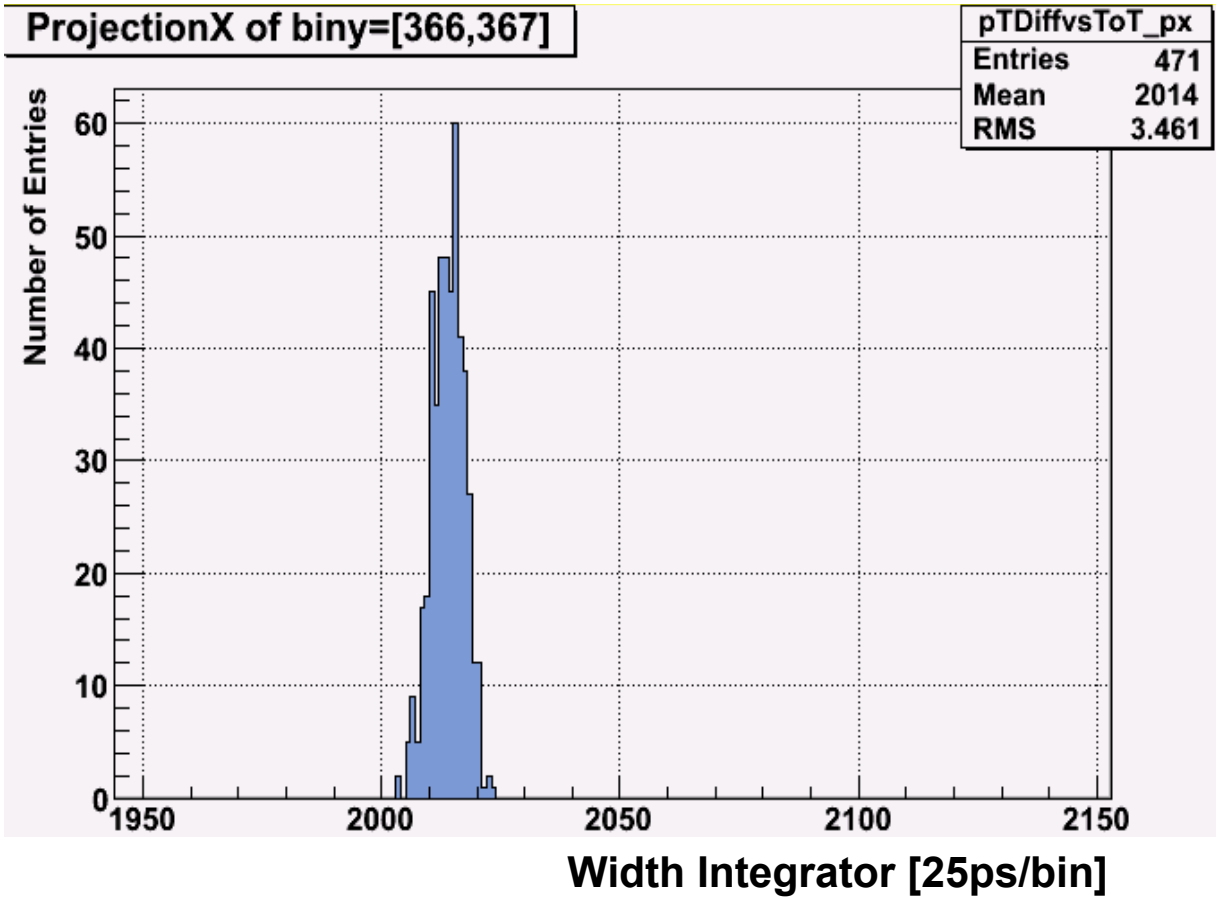


Large jitter of the integrator width (charge)
Due to high gain for low frequency noise

After walk correction via leading edges:
Charge Resolution: **0.17 %**

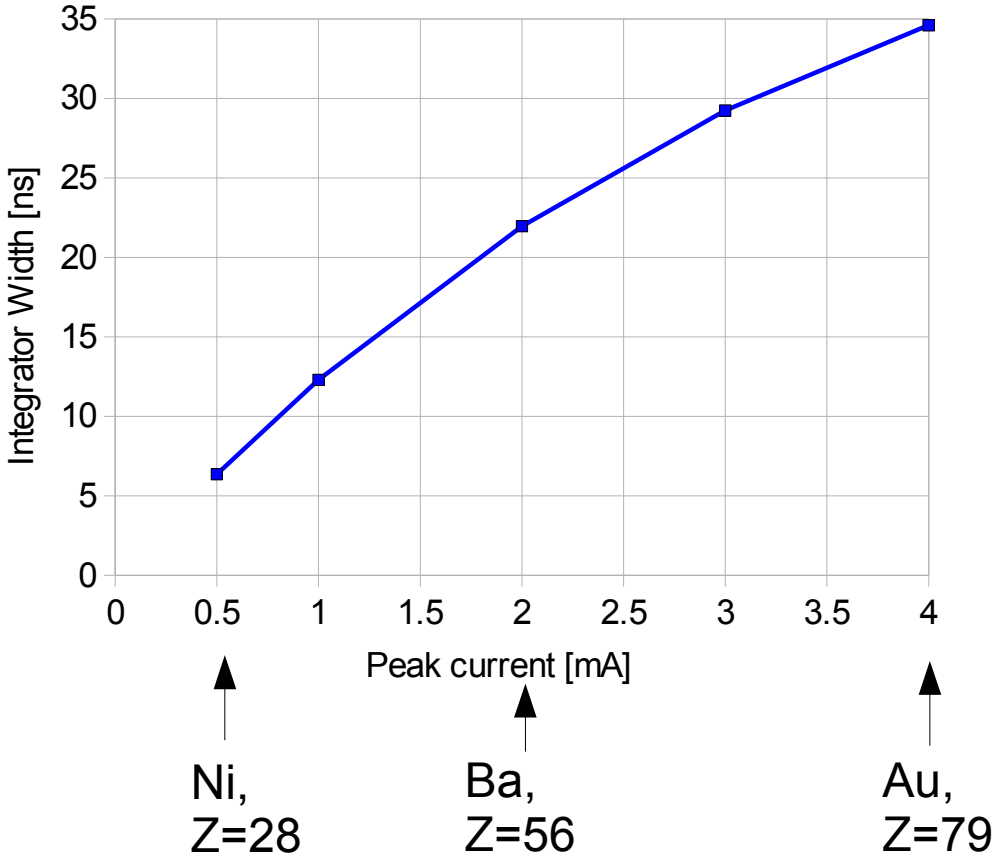
Calorimeter <= 0.1% @ 1GeV
excluding detector performance,
educated guess

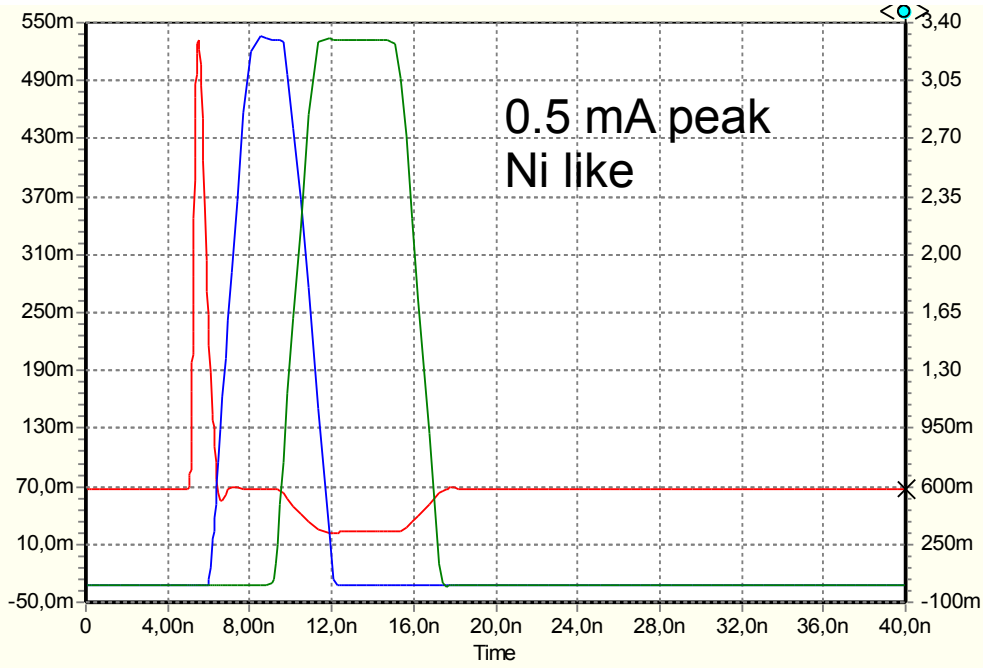
Resolution scales roughly
like Sqrt(charge)

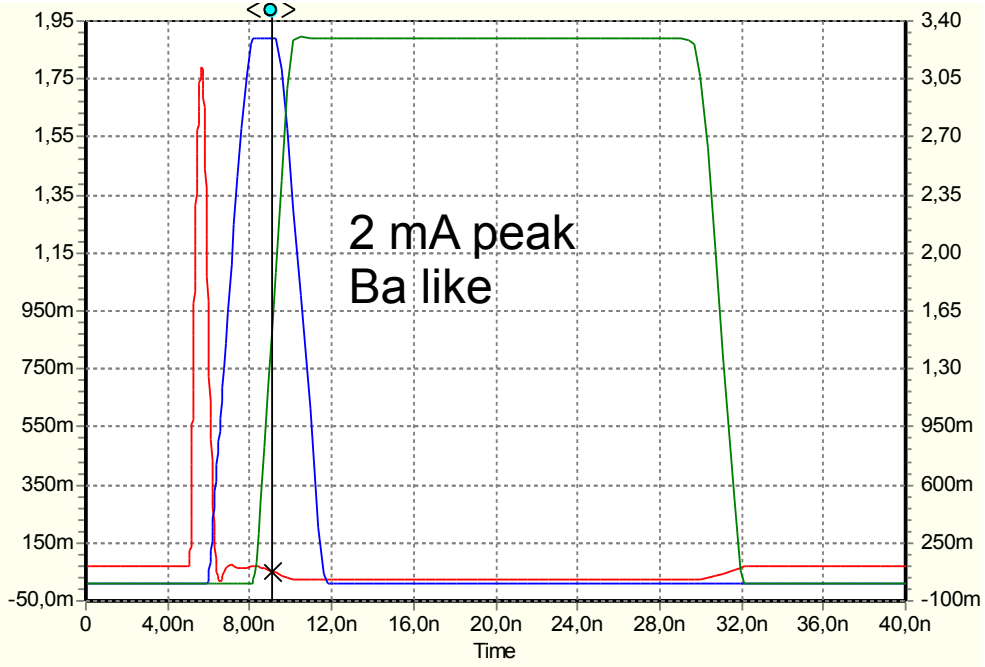


Veto (monocrystalline diamond, 100 um thickness, 8.5 * 8.3 mm^2, 16 x-, 16 y-strips)

Limited dynamic range: factor 10
Resolution: 0.5% in charge (to be verified)





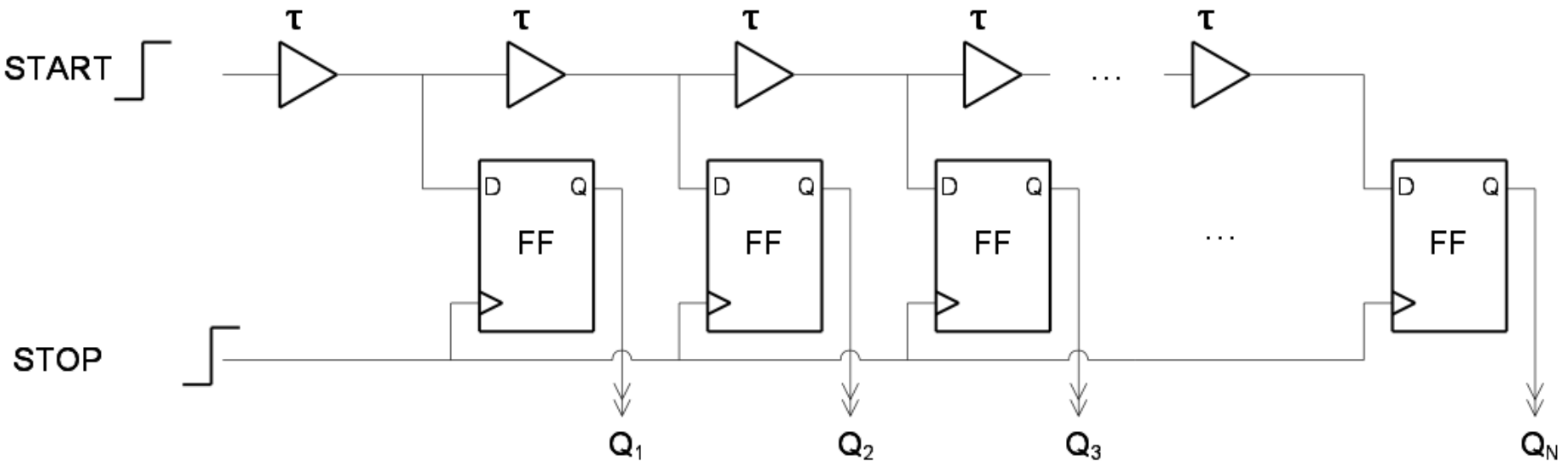


Resolution sufficient to separate Z from Z+1 even up to Uranium (2%)

Radiation Damage ?

TDC in FPGA: Theory

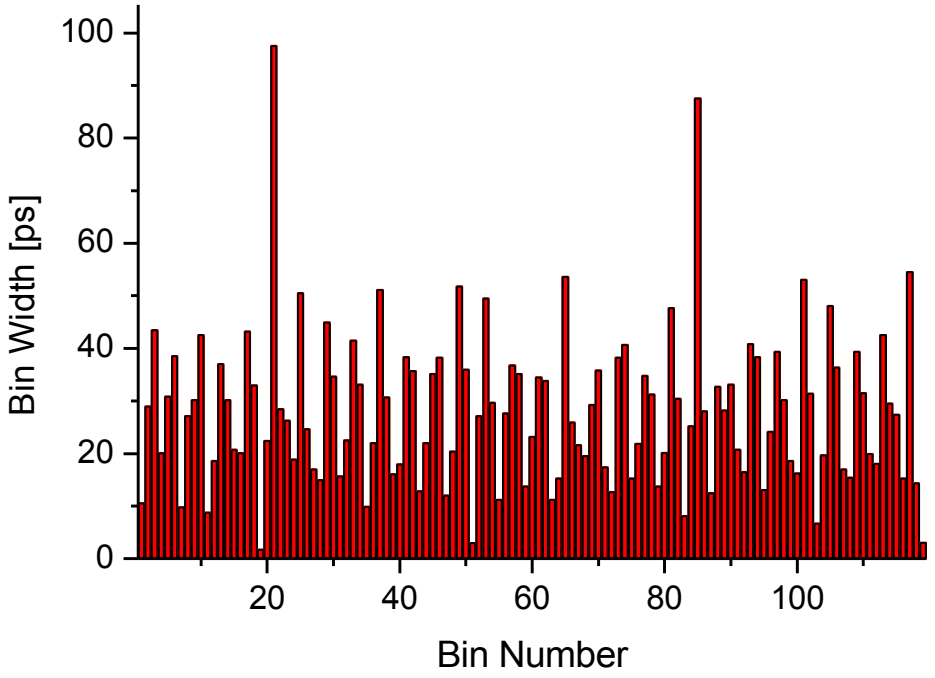
- **Developed, implemented and tested in hardware by Eugen Bayer**
- The used method is very simple! **Tapped Delay Line**
  - The asynchronous input signal (e.g. one rising edge) runs through a chain of delay elements
  - The position of the 0/1 transition is stored in the FF array at the next rising edge of the system clock



Medium size FPGA: several 10000 flip-flops + logic elements

TDC in FPGA (II): Reality

- **The "Carry-Chain" serves as a delay chain**
- **Carry-Chain multiplexers are the delay elements**
- **Delay (max.) = 45 ps (Virtex-4: CIN to COUT = 90 ps)**
- **Real delays vary: cell-by-cell calibration necessary**

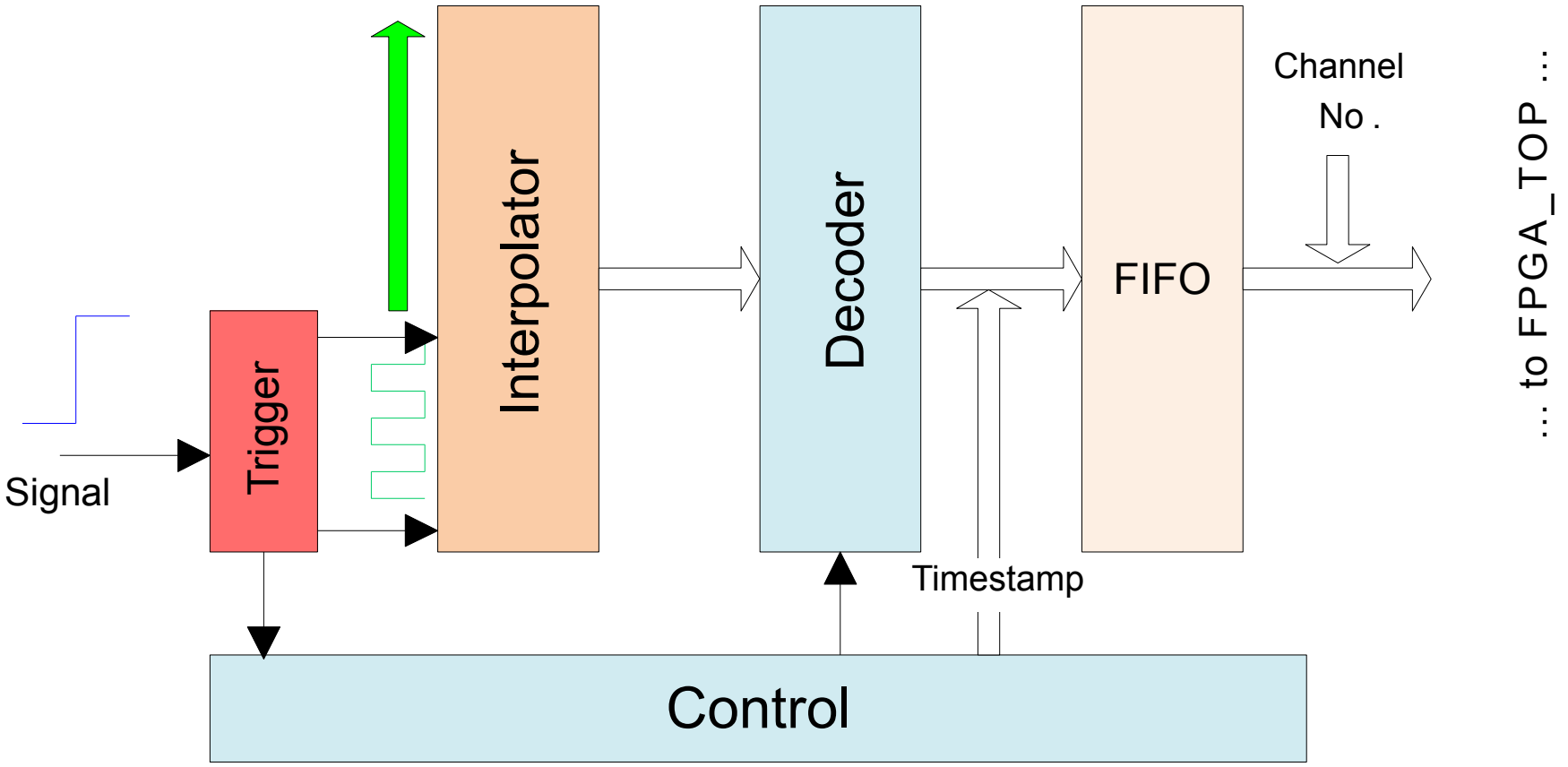


Consequences:

- Bad Differential Non Linearity (DNL) needs calibration (in FPGA or offline)
- Trick to improve resolution: measure several times to “remove” ultra wide bins

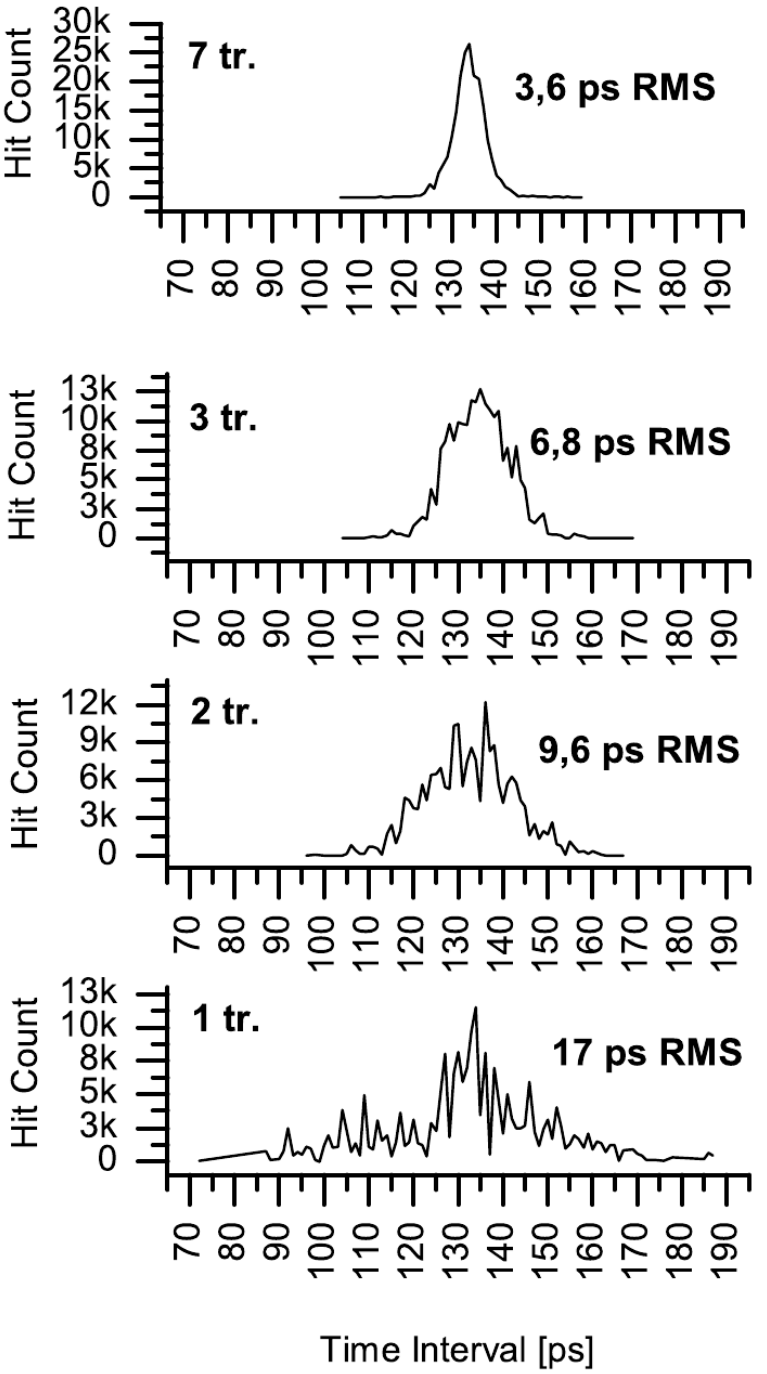
TDC in FPGA : Architecture for Multi-Hit capability

- TDL method extended with “Wave Union” method
- Pipelined design
- Dead time = 15 ns (3 sys-clock cycles)
- Buffer for 512 hits per channel



TDC in FPGA : Results

- TDC time resolution down to 3.6 ps RMS
- No tails
- World record!
- For a large number of channels: RMS ~ 10ps

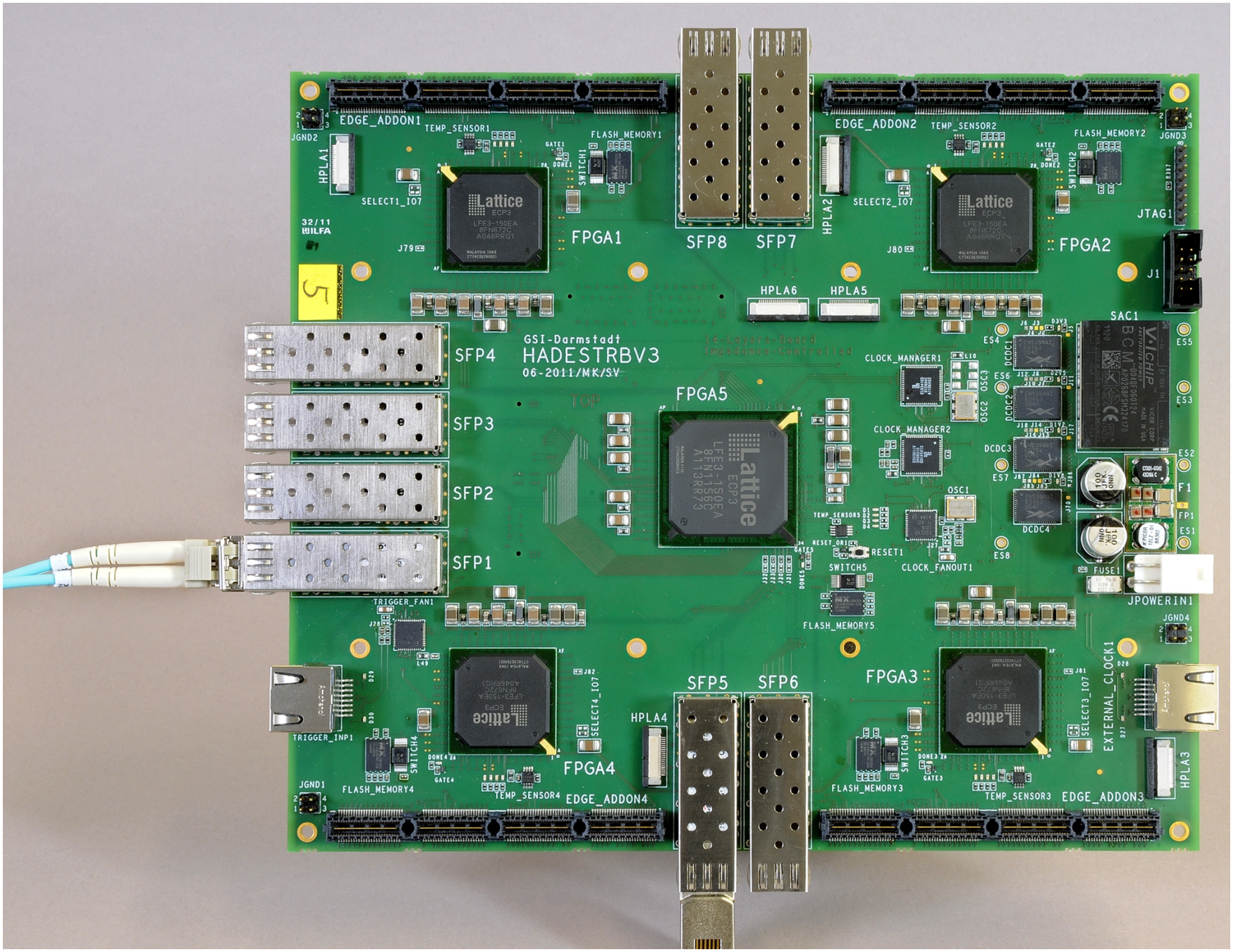


- Temperature dependence: 8 ps / K
- Voltage: ~4 ps for 10 mV supply voltage change

Needs load balancing via dummy activities

- No crosstalk measured (proper PCB design)
- Up to 56 channels on XC4VLX40 with 40k logic cells

FPGA in TDC works extremely well!

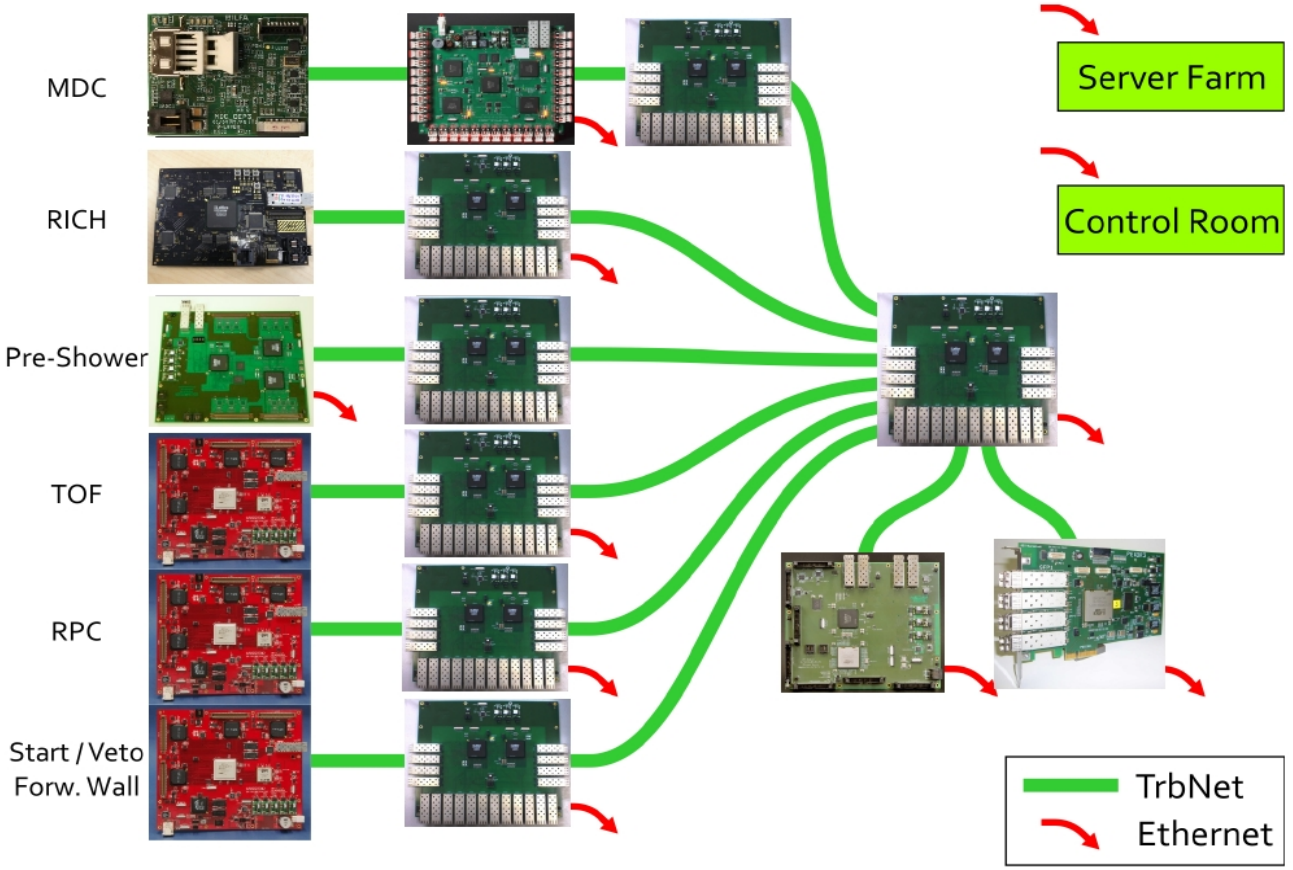


- 4 modern FPGA-TDCs with high pin count (208) connectors (add on boards)
- Low noise power supply (48V)
- Network: 8 times up to 3GBit/s and/or 1GBit/s Ethernet

Hades & the KISS principle

Electronics

- 4,500 PCB's in total
- 1,500 ADC channels (multiplexed from 80,000 signals)
- 30,000 TDC channels



Many elements (~100) / subsystem

Data Rates:

- Up to 100 kHz trigger rate
- 250 MByte/s (average),
  400 MByte/s (peak)

Data transport

- 550 FPGA's
- 1050 optical transceivers
- 7,000 m optical fibre
- 800 m 1-wire & CAN bus
- 32 Ethernet switches
- 15 Gbit/s uplink to Eventbuilders
- 10 Gbit/s uplink to storage

Server farm

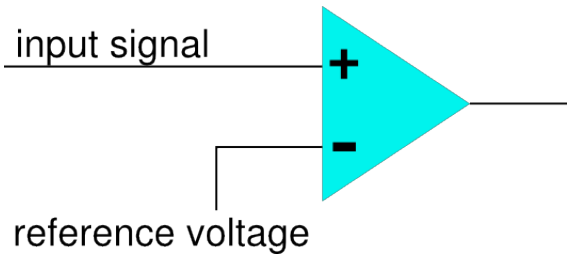
- 160 TB hard disks
- 44 CPU cores
- 100 TB storage / week via Robot

Summary & outlook

Summary:

- New concept for measuring charge with high resolution TDC.
- High rate capability (several MHz)
- New concept for implementing TDC's in FPGA's
- Promising first results
- Not yet there

Outlook:



- Include more of the FEE inside the FPGA:
  - Discriminators –> LVDS receivers
  - DAC's –> integrated logic pulses with variable duty cycle
- Test with real diamond signals in beam

On the way